

WHAT IS CLAIMED IS:

- 1 1. A method for fabricating sidewall spacers in the manufacture of an integrated circuit
2 device, comprising the steps of:
3 providing a substrate having a gate structure formed thereon;
4 forming a dielectric spacer layer over the semiconductor substrate; and
5 etching said dielectric spacer layer, prior to forming a layer subsequent to the
6 dielectric layer, to form L-shaped spacers.

- 1 2. The method of Item 1, further including the step of forming a liner oxide layer over said
2 gate structure prior to the step of forming the dielectric spacer layer.

- 1 3. The method of Item 2 wherein said liner oxide layer is deposited to a thickness of
2 between approximately 20 Angstroms and 200 Angstroms.

- 1 4. The method of Item 1 wherein said dielectric spacer layer comprises a nitride layer.

- 1 5. The method of Item 3, wherein the said dielectric spacer has a thickness in the range of
2 150 Angstroms and 500 Angstroms.

- 1 6. The method of Item 1 wherein said dielectric spacer layer comprises a silicon oxynitride
2 layer.

- 1 7. The method of Item 1 wherein the step of etching said dielectric layer includes
2 anisotropically etching said dielectric layer to form L-shaped spacers, said L-shaped
3 spacers having vertical portions varying in thickness and horizontal portions varying in
4 thickness.

- 1 8. The method of Item 7, wherein said horizontal portion of the L-shaped spacers
2 having bulging profiles varying gradually in thickness from a maximum thickness
3 immediately adjacent the vertical portion of the L-shaped spacer to a portion of the L-
4 shaped spacer furthers from the vertical-portion of the L-shaped spacer, wherein the
5 horizontal portion varies gradually to provide for an average thickness of the L-shaped
6 portion that is 50 to 85 percent of the maximum thickness.
- 1 9. The method of Item 7 wherein said dielectric layer is anisotropically etched using a
2 capacitively coupled plasma etch process with an etching chemistry comprising CH₃F
3 and O₂ in combination with an inert gas to form said L-shaped spacers.
- 1 10. The method of Item 7, wherein said dielectric layer is anisotropically etched using an
2 inductively coupled plasma etch process with an etching chemistry comprising CH₃F
3 and O₂ in combination with an inert gas.
- 1 11. The method of Item 1, wherein the step of etching said dielectric layer to form said L-
2 shaped spacers includes using CH₃F and O₂ chemistry in ratios ranging from
3 approximately 2:1 to approximately 5:1 CH₃F to O₂.
- 1 12. The method of Item 11, wherein the step of etching said dielectric layer to form said L-
2 shaped spacers utilizes a pressure during the etch process ranging from approximately
3 20 milliTorrs to approximately 500 milliTorrs.
- 1 13. The method of Item 11, wherein the step of etching includes using a temperature
2 ranging from approximately 10 degrees C and 30 degrees C.

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1 14. An apparatus comprising a first transistor structure including an L-shaped spacer
2 having a vertical portion varying substantially in thickness over a majority of its length
3 and a horizontal portion varying substantially in thickness over a majority of its length.

1 15. The apparatus of Item 14, wherein said vertical and horizontal portions of L-shaped
2 spacers have a bulging profile which varies gradually in thickness from a maximum
3 thickness immediately adjacent the vertical portion of the L-shaped spacer to a portion
4 of the L-shaped spacer furthest from the vertical-portion of the L-shaped spacer,
5 wherein the horizontal portion varies gradually to provide for an average thickness of
6 the L-shaped portion that is 50 to 85 percent of the maximum thickness.

1 16. The apparatus of Item 14, wherein the length of the horizontal portion of the L-shaped
2 spacer ranges from approximately 80 percent of the deposition thickness to 150
3 percent of the deposition thickness.

1 17. The apparatus of Item 14 further comprising:
2 a second transistor immediately adjacent to the first transistor, where in a distance
3 between a sidewall portion of a gate of the first transistor and a sidewall
4 portion of a gate of the second transistor less than 120 nanometers.

- 1 18. A method for fabricating sidewall spacers in the manufacture of an integrated circuit
2 device, comprising the steps of:
3 providing a substrate having a gate structure formed thereon;
4 forming a liner oxide layer on said gate structure;
5 forming a dielectric spacer layer over said liner oxide layer; and
6 anisotropically etching said dielectric layer, prior to forming a layer subsequent to
7 the dielectric layer, to form L-shaped spacers, said L-shaped spacers having
8 vertical portions and a horizontal portion, wherein the horizontal portion
9 varies gradually in thickness from a maximum thickness immediately
10 adjacent the vertical portion of the L-shaped spacer to a portion of the L-
11 shaped spacer furthest from the vertical-portion of the L-shaped spacer,
12 wherein the horizontal portion varies gradually to provide for an average
13 thickness of the L-shaped portion that is 50 to 85 percent of the maximum
14 thickness.